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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/038,806	01/02/2002	Timothy M. Takeuchi	42P13557	2936

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EXAMINER

VU, QUANG D

ART UNIT

PAPER NUMBER

2811

DATE MAILED: 09/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/038,806

Applicant(s)

TAKEUCHI, TIMOTHY M.

Examiner

Quang D Vu

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on amendment filed on 08/07/03.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 7-26 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 7-26 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- 1) ☐ Certified copies of the priority documents have been received.
  - 2) ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,297,549 to Hiyoshi in view of US Patent No. 5,720,342 to Owens et al., and further in view of US Patent No. 5,397,917 to Ommen et al.

Regarding claim 7, Hiyoshi (figures 2A-F) teaches an apparatus comprising:

a package substrate having top (331) and bottom (332) buildup layers disposed on a ceramic substrate core (31), wherein a portion of the substrate core is exposed at a top surface of the package substrate for attachment of a heat spreader (32, 39, 38).

Hiyoshi teaches a ceramic substrate core (31). Hiyoshi differs in not showing a thermally conductive substrate core. The thermally conductive ceramic substrate is known in the art as shown for example by Owens et al. (column 4, lines 37-41). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to select thermally conductive ceramic substrate, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. In re Leshin, 125 USPQ 416.

Hiyoshi and Owens et al. differ in not showing a package substrate having top and bottom buildup layers including a plurality of conductive traces. However, Ommen et al. (figure 1) teach a top side conductive traces (20) and the bottom side conductive traces (24) that are formed on substrate layer (18) (column 3, line 46 – column 4, line 8). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Ommen et al. into the device taught by Hiyoshi and Owens et al. because it provides connection between the chip and external device.

Regarding claim 8, Hiyoshi teaches the exposed portion of the substrate core (31) extends around the perimeter of the top surface buildup layer (331) (see figure 2A).

Regarding claim 9, Hiyoshi, Owens and Ommen et al. differ in not showing the substrate core is made of metal. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the substrate core is made of metal because it depends on the amount of heat that needs to be dissipate from the chip.

3. Claims 10-15 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,118,177 to Lischner et al. in view of US Patent No. 6,297,549 to Hiyoshi.

Regarding claim 10, Lischner et al. (figure 1) teach an apparatus comprising:  
an integrated circuit (130) having a top surface and a backside surface, the integrated circuit (130) mounted to the package substrate (120) with the top surface of the integrated circuit (130) facing the package substrate (120); and  
a heat spreader (140) mounted to the substrate core (120), a bottom surface of the heat spreader (140) thermally coupled to the backside surface of the integrated circuit (130).

Lischner et al. differ in not showing a package substrate having first portions and second portion, and a buildup layer being disposed on only the first portion of the substrate core. However, Hiyoshi (figures 2A-F) teaches a package substrate (31) including a thermally conductive substrate, having first portions (a portion of area having layers 331 and 332) and second portion (a portion of area without having layers 331 and 332), and a buildup layer (331 or 332) being disposed on only the first portion (a portion of area having layers 331 and 332) of the substrate core (31). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Hiyoshi into the device taught by Lischner et al. because it provides connection between the semiconductor device and the external circuit. The combined device shows a package substrate including a thermally conductive substrate, having first portion and second portion, and a buildup layer being disposed on only the first portion of the substrate core; and a heat spreader mounted to the second portion of the substrate core, a bottom surface of the heat spreader thermally coupled to the backside surface of the integrated circuit.

Regarding claim 11, Lischner et al. teach the heat spreader (140) is thermally coupled to a perimeter portion of the substrate core (120).

Regarding claim 12, Lischner et al. teach the heat spreader (140) is soldered (143) to the substrate core (120).

Regarding claim 13, Lischner et al. teach the heat spreader (140) is made of metal (column 2, lines 64-66).

Regarding claim 14, Lischner et al. and Hiyoshi differ in not showing the substrate core is made of metal. It would have been obvious to one having ordinary skill in the art at the time the

Art Unit: 2811

invention was made for the substrate core is made of metal because it depends on the amount of heat that needs to be dissipate from the chip.

Regarding claim 15, Lischner et al. teach a thermal interface material (142) disposed between the backside surface of the integrated circuit (130) and the bottom surface of the heat spreader (140) (column 2, lines 45-48).

Regarding claim 18, Lischner et al. teach the integrated circuit (130) is mechanically and electrically coupled to the package substrate (120) by a plurality of solder bump interconnections (134).

Regarding claim 19, Lischner et al. teach a printed circuit board (150), wherein the package substrate (120) is mounted on the printed circuit board (150).

Regarding claim 20, Lischner et al. teach the package substrate (120) is mechanically and electrically coupled to the printed circuit board (150) by a plurality of solder bump interconnections (152).

4. Claims 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lischner et al. in view of Hiyoshi, and further in view of US Patent No. 6,229,204 to Hembree.

Regarding claim 16, Lischner et al. and Hiyoshi differ in not showing a heat sink attached to a top surface of the heat spreader. However, Hembree teaches a heat sink (28) attached to a top surface of the heat spreader (30) (see figures 5 and 6). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a heat sink of Hembree into the device taught by Lischner et al. and Hiyoshi since it is desirable to enhance heat dissipation.

Art Unit: 2811

Regarding claim 17, Lischner et al. and Hiyoshi differ in not showing a fan attached to the heat sink. However, Hembree teaches a fan attached to the heat sink (column 4, lines 13-14). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a fan of Hembree into the device taught by Lischner et al. and Hiyoshi since it is desirable to increase heat dissipation.

5. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 4,561,011 to Kohara et al. in view of US Patent No. 6,297,549 to Hiyoshi.

Regarding claim 21, Kohara et al. (figure 5) teach an apparatus comprising: at least two integrated circuits (6) having top surfaces and backside surfaces, the integrated circuits (6) mounted on a first surface of the package substrate (7) with the top surfaces of the integrated circuits (6) facing the package substrate (7); and a heat spreader (16) thermally coupled to an exposed portion of the substrate core (7), wherein a bottom surface of the heat spreader (16) is thermally connected to the backside surfaces of the integrated circuits (6).

Kohara et al. differ from the claimed invention by not showing a package substrate having top and bottom surface buildup layers disposed on a thermally conductive substrate core. However, Hiyoshi (figures 2A-F) teaches a package substrate (31) having first portions (a portion of area having layers 331 and 332) and second portion (a portion of area without having layers 331 and 332), and a buildup layer (331 or 332) being disposed on only the first portion (a portion of area having layers 331 and 332) of the substrate core (31). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a package substrate having top and bottom surface buildup layers of Hiyoshi into the

Art Unit: 2811

device taught Kohara et al. because it provides connection between the semiconductor device and the external circuit. The combined device shows at least two integrated circuit having a top surface and a backside surface, the integrated circuits mounted to the package substrate with the top surface of the integrated circuits facing the package substrate; and a heat spreader mounted to the second portion of the substrate core, a bottom surface of the heat spreader thermally coupled to the backside surface of the integrated circuit.

6. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kohara et al. in view of Hiyoshi, and further in view of US Patent No. 6,215,670 to Khandros.

Regarding claim 22, Kohara et al. and Hiyoshi apply to this claim as discussed regarding claim 21 above.

Kohara et al. and Hiyoshi differ in not showing one or more capacitors mounted on a top surface of the package substrate. However, Khandros teaches one or more capacitors mounted on a top surface of the package substrate (column 12, lines 40-43; lines 48-50). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the capacitors of Khandros into the device taught by Hiyoshi or Kohara et al., since it is desirable to improve electrical performance of semiconductor devices operating at high frequencies.

7. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kohara et al. in view of Hiyoshi, and further in view of US Patent No. 6,118,177 to Lischner et al.



Regarding claim 23, Kohara et al. and Hiyoshi apply to this claim as discussed regarding claim 21 above.

Kohara et al. and Hiyoshi differ in not showing the heat spreader is soldered to the substrate core. However, Lischner et al. (figure 1) teach the heat spreader (140) is soldered (143) to the substrate core (120). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Lischner et al. into the device taught by Hiyoshi because it is securely hold the heat spreader in place.

8. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lischner et al. in view of Hiyoshi, and further in view of US Patent No. 5,397,917 to Ommen et al.

Regarding claim 10, Lischner et al. (figure 1) teach an apparatus comprising:  
an integrated circuit (130) having a top surface and a backside surface, the integrated circuit (130) mounted to the package substrate (120) with the top surface of the integrated circuit (130) facing the package substrate (120); and  
a heat spreader (140) mounted to the substrate core (120), a bottom surface of the heat spreader (140) thermally coupled to the backside surface of the integrated circuit (130).

Lischner et al. differ in not showing a package substrate having first portions and second portion, and a buildup layer being disposed on only the first portion of the substrate core. However, Hiyoshi (figures 2A-F) teaches a package substrate (31) including a thermally conductive substrate, having first portions (a portion of area having layers 331 and 332) and second portion (a portion of area without having layers 331 and 332), and a buildup layer (331 or 332) being disposed on only the first portion (a portion of area having layers 331 and 332) of the

substrate core (31). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Hiyoshi into the device taught by Lischner et al. because it provides connection between the semiconductor device and the external circuit. The combined device shows a package substrate including a thermally conductive substrate, having first portion and second portion, and a buildup layer being disposed on only the first portion of the substrate core; and a heat spreader mounted to the second portion of the substrate core, a bottom surface of the heat spreader thermally coupled to the backside surface of the integrated circuit.

Lischner et al. and Hiyoshi further differ in not showing a package substrate having top and bottom buildup layers including a plurality of conductive traces. However, Ommen et al. (figure 1) teach a top side conductive traces (20) and the bottom side conductive traces (24) that are formed on substrate layer (18) (column 3, line 46 – column 4, line 8). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Ommen et al. into the device taught by Lischner et al. and Hiyoshi because it provides connection between the chip and external device. The combined device shows a package substrate having top and bottom buildup layers including a plurality of conductive traces.

Regarding claim 25, Lischner et al. teach the heat spreader (140) is thermally coupled to a perimeter portion of the substrate core (120).

9. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lischner et al. and Hiyoshi in view of Ommen et al., and further in view of US Patent No. 6,229,204 to Hembree.

Art Unit: 2811

Regarding claim 16, Lischner et al., Hiyoshi and Ommen et al. differ in not showing a heat sink attached to a top surface of the heat spreader. However, Hembree teaches a heat sink (28) attached to a top surface of the heat spreader (30) (see figures 5 and 6). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a heat sink of Hembree into the device taught by Lischner et al., Hiyoshi and Ommen et al. since it is desirable to enhance heat dissipation.

### ***Response to Arguments***

10. Applicant's arguments with respect to claims 7-23 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 703-305-3826. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

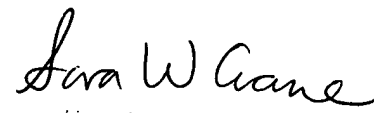
Application/Control Number: 10/038,806

Page 11

Art Unit: 2811

qv

September 4, 2003

A handwritten signature in black ink, reading "Sara W. Crane". The signature is written in a cursive style with a large initial "S" and a long, sweeping underline.

Sara Crane  
Primary Examiner